Multi-Stage Network Processor for an Independent HVDC Grids Supervisory Control

Davood Babazadeh
KTH – Royal Institute of Technology
Stockholm Sweden
Outline

• Introduction to HVDC grid
• HVDC supervisory grid control
  – Architecture
  – Application
• Network processor
• Simulation and result
• Conclusion
New needs in Power System

- Global Electricity demand will increase by more than 70 percent by 2035 (IEA)
- Growth in sustainable energy from 20 to 31%
  - Offshore wind
  - Remote solar
- Increases in power trade across national borders
Solutions

- Overlaying UHVAC grid
  - get permission to build new overhead lines
  - Line transmission limit
  - Synchronized interconnected areas

- HVDC Grid
  - DC transmission line less costly per length than an equivalent AC
  - Relevant offshore solution
  - Power loss reduction
  - Increased power capacity vs. AC
  - Less visual impact
HVDC Grid Challenges

- DC fault protection
- Operational voltage level
- Standardization for converter station design
- Multiple-vendor interoperability
- Multiple-TSO operation (ENTSOE)
- Control center application
  - State Estimation
  - Topology processor
  - Control mode assignment
  - Power injection control
  - Ancillary service such as multi-area frequency support
HVDC Grid Control Hierarchy

- AC / DC grid operation
  - Combined AC/DC OPF
  - Economic consideration

- DC Grid Coordination

- Outer Control
  - DC voltage
  - Power
  - Droop

- Current Control Loop

- Valve Switching

- Local Control

- Global Control

- Time scales:
  - us ~ ms
  - ~100 ms
  - sec ~ 1 min
  - 15 min
Primary Control in HVDC Grid

- Power disturbance in HVDC grid
- DC Voltage changes (not unique indication same as frequency in ac)
- Voltage deviations are dependant on network topology
- Some nodes to compensate the power change by controlling DC voltage

Need of Supervisory Controller
- To choose proper control mode
- Coordinate the converters set-points
HVDC Grid Coordination

- Real time power balancing in the DC grid
- Control mode assignment
  - DC slack converter (or droop control) for real time mismatches
- Tracking connecting AC area’s schedule
- DC grid contingency management
- Ancillary service coordination
DC Grid Control Architecture/ Responsibilities

- (a) Independent HVDC operator
- (b) Integrated AC/HVDC TSO
- (c) Distributed among AC TSOs
HVDC Supervisory Control

- State estimation
  - DC measurement
- Network processor
  - Topology processor
  - Island detection
  - Control mode assignation
- Control applications
  - Power injection control
  - Ancillary service such as multi-area frequency support
DC Supervisory injection control problem can be formulated as a nonlinear constrained optimization problem.

\[
\begin{align*}
    f(x) \\
    \text{s.t.} \\
    g(x) &= b_{eq} \\
    b_{ineq1} &\leq h(x) \leq b_{ineq2} \\
    LB &\leq x \leq UB
\end{align*}
\]

The state variables are

\[
x = \begin{bmatrix} U \\ I \\ P_{dc} \end{bmatrix}
\]

**Prerequisite**
- Network Topology
- Islanding
- Control mode assignment

D. Babazadeh, D. Van Hertem, M. Rabbat, L. Nordström "Coordination of Power Injection in HVDC Grids with Multi-TSOs and Large Wind Penetration" IET AC/DC 2015
Network Processor

• **Topology processor**
  – Breaker status
  – Islands detection (global info)
  – Centralized or two-level approach

• **Control mode assignment**
  – What is the proper metric for operator?
  – Converter capacity (local info)
  – AC area power schedule (global info)
  – Grid characteristics and capability (local info)
Multi Stage Architecture

- Less information to higher level
- Less computational complexity
- Useful info for local operator

<table>
<thead>
<tr>
<th>Substation</th>
<th>Bus</th>
<th>Line</th>
<th>Converter</th>
<th>Grid char.</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>1</td>
<td>0</td>
<td>44</td>
<td>XX</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>24</td>
<td>0</td>
<td>--</td>
</tr>
<tr>
<td>4</td>
<td>2</td>
<td>45</td>
<td>0</td>
<td>--</td>
</tr>
<tr>
<td>4</td>
<td>2</td>
<td>46</td>
<td>0</td>
<td>--</td>
</tr>
<tr>
<td>4</td>
<td>2</td>
<td>47</td>
<td>0</td>
<td>--</td>
</tr>
</tbody>
</table>

Output
- Number of logical DC buses
- Connecting line and converters
- Control mode metric

Measurements
- Power
- Voltage, Current (PCC)
- Breaker status
Local Processor

**OPERATIONAL**
- Substation Analysis
- Connectivity Analysis
- Read the breakers’ status
- Connected AC grid characteristic
- Design Matrix building
- Read the substation’s measurement
- Start

**Output**
- Number of logical DC buses
- Connecting line and converters
- Control mode metric

**Measurements**
- Power
- Voltage, Current (PCC)
- Breaker status

**Central Processor**
- List of Islands
- Admittance Matrix
- Control mode selection

**Local Processor**

![Diagram of Local Processor and Central Processor interaction]

![Diagram of Connected AC grid characteristic]

**List of Islands Admittance Matrix Measurements**
- Power
- Voltage, Current (PCC)
- Breaker status

**VSC**
- VSC 2
- VSC
- Grid
Local Processor – Design Flowchart

Design Matrix

- Information about the connectivity
- DM(i;j) shows the different paths connecting vertex i with vertex j
  - From adjacent matrix and cofactor matrix
- Function of the status of the breakers

\[
DM (1;3) = e1 + e6e10e5 + e6e9e4 + e6e8e3 + e6e7e2
\]
Connectivity Matrix

- $\text{Con}(i;j)$ contains 1 if vertex $i$ is connected to vertex $j$

$$\text{status} = \begin{bmatrix} 1 & 1 & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 \end{bmatrix}$$

$$\text{Con} = \begin{bmatrix}
  1 & 0 & 1 & 1 & 0 & 0 & 0 & 1 & v1 \\
  0 & 1 & 0 & 0 & 1 & 1 & 1 & 0 & v2 \\
  1 & 0 & 1 & 1 & 0 & 0 & 0 & 1 & v3 \\
  1 & 0 & 1 & 1 & 0 & 0 & 0 & 1 & v4 \\
  0 & 1 & 0 & 0 & 1 & 1 & 1 & 0 & v5 \\
  0 & 1 & 0 & 0 & 1 & 1 & 1 & 0 & v6 \\
  0 & 1 & 0 & 0 & 1 & 1 & 1 & 0 & v7 \\
  1 & 0 & 1 & 1 & 0 & 0 & 0 & 1 & v8 
\end{bmatrix}$$
Local Processor – Operational flowchart

Start

Read the substation’s measurement

Design Matrix building

Read the breakers’ status

Connectivity Analysis

Substation Analysis

End

Substation Matrix

• Bus/branch model of the entire substation

<table>
<thead>
<tr>
<th>Substation</th>
<th>Bus</th>
<th>Line</th>
<th>Converter</th>
<th>Grid char.</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>1</td>
<td>0</td>
<td>44</td>
<td>XX</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>24</td>
<td>0</td>
<td>--</td>
</tr>
<tr>
<td>4</td>
<td>2</td>
<td>45</td>
<td>0</td>
<td>--</td>
</tr>
<tr>
<td>4</td>
<td>2</td>
<td>46</td>
<td>0</td>
<td>--</td>
</tr>
<tr>
<td>4</td>
<td>2</td>
<td>47</td>
<td>0</td>
<td>--</td>
</tr>
</tbody>
</table>
• Build the Adjacent Matrix of the Network
• Islands
• Assign a slack bus in each island for centralized DC slack control scheme

Topology Processor – Central Level

Start

Read the inputs

SM updating

Adjacent Matrix

Islanding check

End

List of Islands
Admittance Matrix
Control mode selection

Central Processor

Output
• Number of logical DC buses
• Connecting line and converters
• Control mode metric

Measurements
• Power
• Voltage, Current (PCC)
• Breaker status

Local Processor

Grid
Central Processor – Algorithm Flowchart

Substation Matrix Updating
- Give a unique number to each bus, according to the Position vector
  - Pos_vec(i) = 0 if the position is available
- Add a new column with the new number of the bus

Substation Matrix – Sub 3

<table>
<thead>
<tr>
<th>Substation</th>
<th>Bus</th>
<th>Line</th>
<th>Converter</th>
<th>Bus New n</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>1</td>
<td>0</td>
<td>3</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>23</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Adjacent Matrix
- Build the Adjacent Matrix of the Network
- \( A(i;j) = 1 \) if buses (new number) \( i \) and \( j \) are connected by a line
- \( Y \) matrix
Central Processor – Algorithm Flowchart

Laplacian Matrix
• Number of zero eigenvalues = number of islands
• Eigenvectors: information about islands’ components

Clustering
• Project first 2 non-trivial eigenvectors into the Cartesian space
• The elements corresponding to connected buses form clusters

<p>| | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>-0.5774</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>-0.5774</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>-0.5774</td>
<td></td>
</tr>
<tr>
<td>0.5</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>0.5</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>0.5</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>0.5</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

2 zero eigenvalues
2 clusters
Central Processor – Algorithm Flowchart

Start → Read the inputs → SM updating → Adjacent Matrix → Islanding check → End

![Algorithm Flowchart](image)

### Island 1

<table>
<thead>
<tr>
<th>Substation</th>
<th>Bus New n</th>
<th>Converter</th>
<th>Control index</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>4</td>
<td>4</td>
<td>X</td>
</tr>
<tr>
<td>5</td>
<td>5</td>
<td>5</td>
<td>XXX</td>
</tr>
<tr>
<td>6</td>
<td>6</td>
<td>6</td>
<td>X</td>
</tr>
<tr>
<td>7</td>
<td>7</td>
<td>7</td>
<td>XX</td>
</tr>
</tbody>
</table>

### Island 2

<table>
<thead>
<tr>
<th>Substation</th>
<th>Bus New n</th>
<th>Converter</th>
<th>Control index</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>2</td>
<td>XX</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>3</td>
<td>X</td>
</tr>
</tbody>
</table>
Real-Time Co-Simulation Test-bed

- Co-simulation platform to model the HVDC grid and overlay ICT infrastructure in real time

- OPAL-RT simulator
- OPNET-SITL
- Industrial HVDC controller
- SoftPMU
- DC Measurement Unit

Test case - Islanding

<table>
<thead>
<tr>
<th>Time</th>
<th>Event</th>
</tr>
</thead>
<tbody>
<tr>
<td>40sec</td>
<td>Line L24 and L34 are disconnected due to a fault</td>
</tr>
<tr>
<td>20 - 250 sec</td>
<td>Generation varies at VSC 1</td>
</tr>
<tr>
<td>250 - 400 sec</td>
<td>Generation varies at VSC 6</td>
</tr>
</tbody>
</table>
Islanding

Island A

Island B

PCC Active Power (MW)

Time (s)

VSC 1

VSC 2

VSC 3

VSC 4

VSC 5

VSC 6

VSC 7

0 50 100 150 200 250 300 350 400

0 20 40 60 80 100

0 20 40 60 80 100

System A

System B
Conclusion

- HVDC grid coordinator for optimal real time balancing
- Needs of new application such as control mode assignment within the “Network processor” context.
- Multi-stage network processor can reduce the complexity of required data needed to be sent to DC supervisory control
Thank you

Davood Babazadeh
davood@kth.se