The 13th International Workshop on Electric Power Control Centers
Bled, Slovenia, May 17-20, 2015

Multi-Stage Network Processor for an Independent and Integrated HVDC grid Supervisory Control Architecture

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Abstract

Increasing the integration of renewable energy resources has introduced new requirements to the structure of electric power transmission grids. In addition to distributed renewable production, electric power exchange between neighboring countries also leads to development of transmission grids. Since AC grid solution is limited by legislative issues and long distance transmission capacity, High Voltage Direct Current (HVDC) technology with its different benefits compared to AC such as lower power losses, controllability and visual impact is being considered as appropriate alternative solution. Different aspects of HVDC technology from technical and economic challenges regarding the selection of proper HVDC grid topology to detailed control schemes are addressed extensively in the literature.

Regarding the control of HVDC grids, the concept of centralized DC slack converter has been presented with the task to control the DC voltage level of the grid within the defined value and keep DC power flow in the grid balanced in real-time. Beside the centralized DC slack concept, a distributed DC slack concept called DC voltage droop is proposed and investigated. Similar to primary frequency control in AC grid, the controller uses the local DC voltage deviation as indication of power mismatch and tune the power production based on this local signal. An alternative agent-based control scheme has been also proposed to coordinate the power sharing in HVDC grids.

On top of this fast control design, a supervisory controller is needed to guarantee the optimal operation of the HVDC grid in normal or abnormal states. This supervisory controller can be integrated to available AC Supervisory Control and Data Acquisition (SCADA) in the case of HVDC grid embedded in a single AC area. When it comes to HVDC grid connecting different AC areas, an "*independent HVDC SCADA"* can be defined which coordinates with connecting AC areas' SCADA or it again can be integrated to one of the AC Area's SCADA system called "*integrated HVDC SCADA*".

Regardless of system operation architecture, in order to monitor and operate the HVDC grid, supervisory control needs to be equipped with state estimation including the topology processor. Topology processor uses the real-time circuit breaker status within the substation to determine the system level topology. In the case of HVDC grid, the importance of such topology processor is bolder when it comes to detection of different islands. The islanding case should be recognized as real-time as possible in order to assign the DC slack bus, if not available in the island. In the literature, different algorithms and challenges have been investigated for topology analysis in the context of AC

grid. This includes presentation artificial intelligence methods (e.g. artificial neural network) or integration of Phasor Measurement Unit (PMU) information in the process. Considering the future attentions toward overlay or interconnecting HVDC grid, the similar detailed methodology for HVDC grid with particular challenges seems to be vital.

This work presents a multi-stage network processor as part of independent supervisory control in HVDC grid connecting or overlaying AC areas which can be extended to integrated supervisory control architecture. The proposed approach consists of two levels: 1) process of AC or DC substation topology locally and 2) the secondary process at HVDC grid central supervisory controller. At the substation level, the local topology processor determines the branch/bus model of the substation including the possible standalone HVDC converter using breaker status in the form of *support matrix* which is the combination of *substation matrix* and *standing alone matrix*. Substation Matrix holds information regarding this simplified substation model and the lines connected to it and number of logical buses/vertexes per substation. Standing alone matrix is created when the converter in the substation is not connected to DC grid and just standing alone. This can be useful for operator for starting the SVC functionality of the VSC stations. The same analysis is performed on all the substations locally and then the support matrices are sent to the network processor at SCADA level.

At central level, the processor creates the general adjacent matrix based on the support matrix of the substations for whole HVDC grid to form the admittance matrix (Y). For the islanding analysis, the corresponding *Laplacian Matrix* is built from the adjacent matrix and clustering method is used to analysis the corresponding Eigen vectors of the Laplacian matrix. Besides, an extended version of current algorithm has been studied and presented for the integrated HVDC supervisory control architecture in which one AC area is responsible for the operation of HVDC grid.